What is claimed is:

1. A display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising:

first to (M+N)th (M and N are positive integers) shift register blocks;

a data input control circuit which controls input of the gray-scale data supplied to the first to (M+N)th shift register blocks;

first to (M+N)th data mask circuits which generate first to (M+N)th gray-scale data by performing mask control for the gray-scale data supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th gray-scale data; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to the first to (M+N)th gray-scale data, the first to (M+N)th gray-scale data being held in the first to (M+N)th shift register blocks,

wherein the first to Mth shift register blocks are disposed in a region on a first direction side of the data input control circuit, shift a given data enable signal input to the first shift register block and output the shifted data enable signal to a shift register block adjacent in a second direction opposite to the first direction, and hold the first to Mth gray-scale data based on the shifted data enable signal,

wherein the (M+1)th to (M+N)th shift register blocks are disposed in a region on the second direction side of the data input control circuit, shift a data enable signal input to the (M+1)th shift register block from the Mth shift register block and output the shifted data enable signal to a shift register block adjacent in the second direction, and hold the (M+1)th to (M+N)th gray-scale data based on the shifted data enable signal,

wherein the first to Mth data mask circuits are connected in the second direction in order from the first to Mth data mask circuit and mask the first to Mth gray-scale data in order from the first to Mth data mask circuit, and

wherein the (M+1)th to (M+N)th data mask circuits are connected in the second

direction in order from the (M+1)th to (M+N)th data mask circuit and unmask the (M+1)th to (M+N)th gray-scale data in order from the (M+1)th to (M+N)th data mask circuit.

2. The display driver circuit as defined in claim 1, further comprising:

first to (M+N)th data mask control circuits which generate first to (M+N)th data mask control signals for performing mask control for the first to (M+N)th gray-scale data,

wherein an ath ($1 \leq a \leq M$; a is an integer) data mask control circuit generates an ath data mask control signal based on a data enable signal output from an ath shift register block, and

wherein a bth ($M+1 \leq b \leq M+N$; b is an integer) data mask control circuit generates a bth data mask control signal based on a data enable signal output from a (b-1)th shift register block.

3. The display driver circuit as defined in claim 2,

wherein a cth ($1 \leq c \leq M+N$; c is an integer) shift register block shifts a data enable signal in the first direction and holds a cth gray-scale data based on the data enable signal shifted in the first direction, when a given shift signal is at a first level,

wherein the cth shift register block shifts a data enable signal in the second direction and holds the cth gray-scale data based on the data enable signal shifted in the second direction, when the shift signal is at a second level, and

wherein a cth data mask control circuit generates a cth data mask control signal according to the level of the shift signal.

4. The display driver circuit as defined in claim 1, further comprising:

a clock input control circuit which controls input of a clock signal which is

supplied to each of the first to (M+N)th shift register blocks and determines shift timing of a data enable signal; and

first to (M+N)th clock mask circuits which generate first to (M+N)th clock signals by performing mask control for the clock signal supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th clock signals,

wherein the first to Mth shift register blocks are disposed in the region on the first direction side of the clock input control circuit and shift a data enable signal based on the first to Mth clock signals,

wherein the (M+1)th to (M+N)th shift register blocks are disposed in the region on the second direction side of the clock input control circuit and shift a data enable signal based on the (M+1)th to (M+N)th clock signals,

wherein the first to Mth clock mask circuits are connected in the second direction in order from the first to Mth clock mask circuit and mask the first to Mth clock signals in order from the first to Mth clock mask circuit, and

wherein the (M+1)th to (M+N)th clock mask circuits are connected in the second direction in order from the (M+1)th to (M+N)th clock mask circuit and unmask the (M+1)th to (M+N)th clock signals in order from the (M+1)th to (M+N)th clock mask circuit.

5. The display driver circuit as defined in claim 4, further comprising:

first to (M+N)th clock mask control circuits which generate first to (M+N)th clock mask control signals for performing mask control for the first to (M+N)th clock signals,

wherein a dth ($1 \leq d \leq M$; d is an integer) clock mask control circuit generates a dth clock mask control signal based on a data enable signal output from a dth shift register block, and

wherein an eth ($M+1 \leq e \leq M+N$; e is an integer) clock mask control circuit

generates an eth clock mask control signal based on a data enable signal output from an (e-1)th shift register block.

6. The display driver circuit as defined in claim 5,

wherein an fth ($1 \leq f \leq M+N$; f is a positive integer) shift register block shifts a data enable signal in the first direction and holds an fth gray-scale data based on the data enable signal shifted in the first direction, when a given shift signal is at a first level,

wherein the fth shift register block shifts a data enable signal in the second direction and holds the fth gray-scale data based on the data enable signal shifted in the second direction, when the shift signal is at a second level, and

wherein an fth clock mask control circuit generates an fth clock mask control signal according to the level of the shift signal.

7. A display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising:

first to (M+N)th (M and N are positive integers) shift register blocks;

a clock input control circuit which controls input of a clock signal which is supplied to each of the first to (M+N)th shift register blocks and determines shift timing;

first to (M+N)th clock mask circuits which generate first to (M+N)th clock signals by performing mask control for the clock signal supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th clock signals; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to first to (M+N)th gray-scale data, the first to (M+N)th gray-scale data being held in the first to (M+N)th shift register blocks,

wherein the first to Mth shift register blocks are disposed in a region on a first direction side of the clock input control circuit, shift a given data enable signal input to

the first shift register block based on the first to Mth clock signals and output the shifted data enable signal to a shift register block adjacent in a second direction opposite to the first direction, and hold the first to Mth gray-scale data based on the shifted data enable signal,

wherein the (M+1)th to (M+N)th shift register blocks are disposed in a region on the second direction side of the clock input control circuit, shift a data enable signal input to the (M+1)th shift register block from the Mth shift register block based on the (M+1)th to (M+N)th clock signals and output the shifted data enable signal to a shift register block adjacent in the second direction, and hold the (M+1)th to (M+N)th gray-scale data based on the shifted data enable signal,

wherein the first to Mth clock mask circuits are connected in the second direction in order from the first to Mth clock mask circuit and mask the first to Mth clock signals in order from the first to Mth clock mask circuit, and

wherein the (M+1)th to (M+N)th clock mask circuits are connected in the second direction in order from the (M+1)th to (M+N)th clock mask circuit and unmask the (M+1)th to (M+N)th clock signals in order from the (M+1)th to (M+N)th clock mask circuit.

8. A display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising:

first to Mth (M is a positive integer) shift register blocks;

a data input control circuit which controls input of the gray-scale data supplied to the first to Mth shift register blocks;

first to Mth data mask circuits which generate first to Mth gray-scale data by performing mask control for the gray-scale data supplied to the first to Mth shift register blocks and output the first to Mth gray-scale data, first to Mth gray-scale data being held in the first to Mth shift register blocks; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to the first to Mth gray-scale data,

wherein the first to Mth shift register blocks are disposed in a region on a first direction side of the data input control circuit, shift a given data enable signal input to the first shift register block and output the shifted data enable signal to a shift register block adjacent in a second direction opposite to the first direction, and hold the first to Mth gray-scale data, for which mask control is performed by the first to Mth data mask circuits, based on the shifted data enable signal, and

wherein the first to Mth data mask circuits are connected in the second direction in order from the first to Mth data mask circuit and mask the first to Mth gray-scale data in order from the first to Mth data mask circuit.

9. A display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising:

first to Nth (N is a positive integer) shift register blocks;

a data input control circuit which controls input of the gray-scale data supplied to the first to Nth shift register blocks;

first to Nth data mask circuits which generate first to Nth gray-scale data by performing mask control for the gray-scale data supplied to the first to Nth shift register blocks and output the first to Nth gray-scale data, the first to Nth gray-scale data being held in the first to Nth shift register blocks; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to the first to Nth gray-scale data,

wherein the first to Nth shift register blocks are disposed in a region on a second direction side of the data input control circuit, shift a given data enable signal input to the first shift register block and output the shifted data enable signal to a shift register block adjacent in the second direction, and hold the first to Nth gray-scale data, for

which mask control is performed by the first to Nth data mask circuits, based on the shifted data enable signal, and

wherein the first to Nth data mask circuits are connected in the second direction in order from the first to Nth data mask circuit and unmask the first to Nth gray-scale data in order from the first to Nth data mask circuit.

10. A display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising:

first to Mth (M is a positive integer) shift register blocks;

a clock input control circuit which controls input of a clock signal which is supplied to each of the first to Mth shift register blocks and determines shift timing;

first to Mth clock mask circuits which generate first to Mth clock signals by performing mask control for the clock signal supplied to the first to Mth shift register blocks and output the first to Mth clock signals; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to first to Mth gray-scale data,

wherein the first to Mth shift register blocks are disposed in a region on a first direction side of the clock input control circuit, shift a given data enable signal input to the first shift register block based on the first to Mth clock signals and output the shifted data enable signal to a shift register block adjacent in a second direction opposite to the first direction, and hold the first to Mth gray-scale data based on the shifted data enable signal, and

wherein the first to Mth clock mask circuits are connected in the second direction in order from the first to Mth clock mask circuit and mask the first to Mth clock signals in order from the first to Mth clock mask circuit.

11. A display driver circuit which drives signal electrodes of a display device

based on gray-scale data, comprising:

first to Nth (N is a positive integer) shift register blocks;

a clock input control circuit which controls input of a clock signal which is supplied to each of the first to Nth shift register blocks and determines shift timing;

first to Nth clock mask circuits which generate first to Nth clock signals by performing mask control for the clock signal supplied to the first to Nth shift register blocks and output the first to Nth clock signals; and

a signal electrode driver circuit which drives the signal electrodes by using drive voltages corresponding to first to Nth gray-scale data,

wherein the first to Nth shift register blocks are disposed in a region on a second direction side of the clock input control circuit, shift a given data enable signal input to the first shift register block based on the first to Nth clock signals and output the shifted data enable signal to a shift register block adjacent in the second direction, and hold the first to Nth gray-scale data based on the shifted data enable signal, and

wherein the first to Nth clock mask circuits are connected in the second direction in order from the first to Nth clock mask circuit and unmask the first to Nth clock signals in order from the first to Nth clock mask circuit.

12. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 1 which drives the signal electrodes based on the gray-scale data.

13. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal

electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 7 which drives the signal electrodes based on the gray-scale data.

14. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 8 which drives the signal electrodes based on the gray-scale data.

15. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 9 which drives the signal electrodes based on the gray-scale data.

16. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 10 which drives the signal electrodes based on the gray-scale data.

17. A display device comprising:

pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 11 which drives the signal electrodes based on the gray-scale data.

18. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 1 which drives the signal electrodes based on the gray-scale data.

19. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 7 which drives the signal electrodes based on the gray-scale data.

20. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 8 which drives the signal electrodes based on the gray-scale data.

21. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 9 which drives the signal electrodes based on the gray-scale data.

22. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 10 which drives the signal electrodes based on the gray-scale data.

23. A display device comprising:

a display panel including pixels specified by a plurality of scan electrodes and a plurality of signal electrodes which intersect each other;

a scan electrode driver circuit which drives the scan electrodes; and

the display driver circuit as defined in claim 11 which drives the signal electrodes based on the gray-scale data.